

Fig. 1

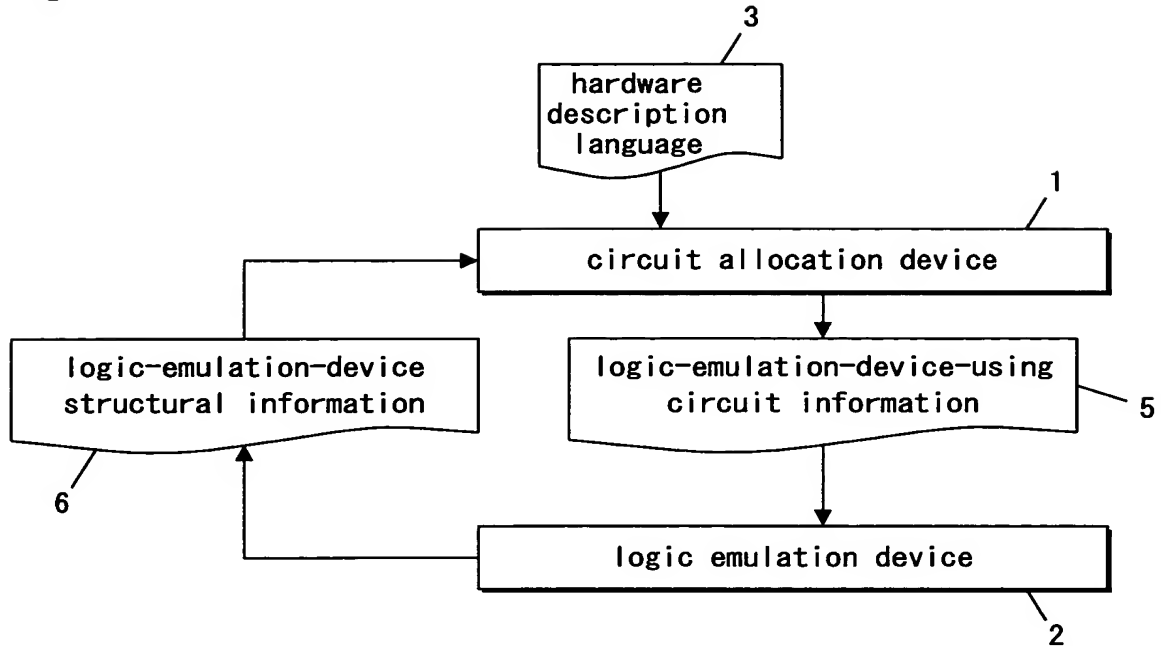


Fig. 2

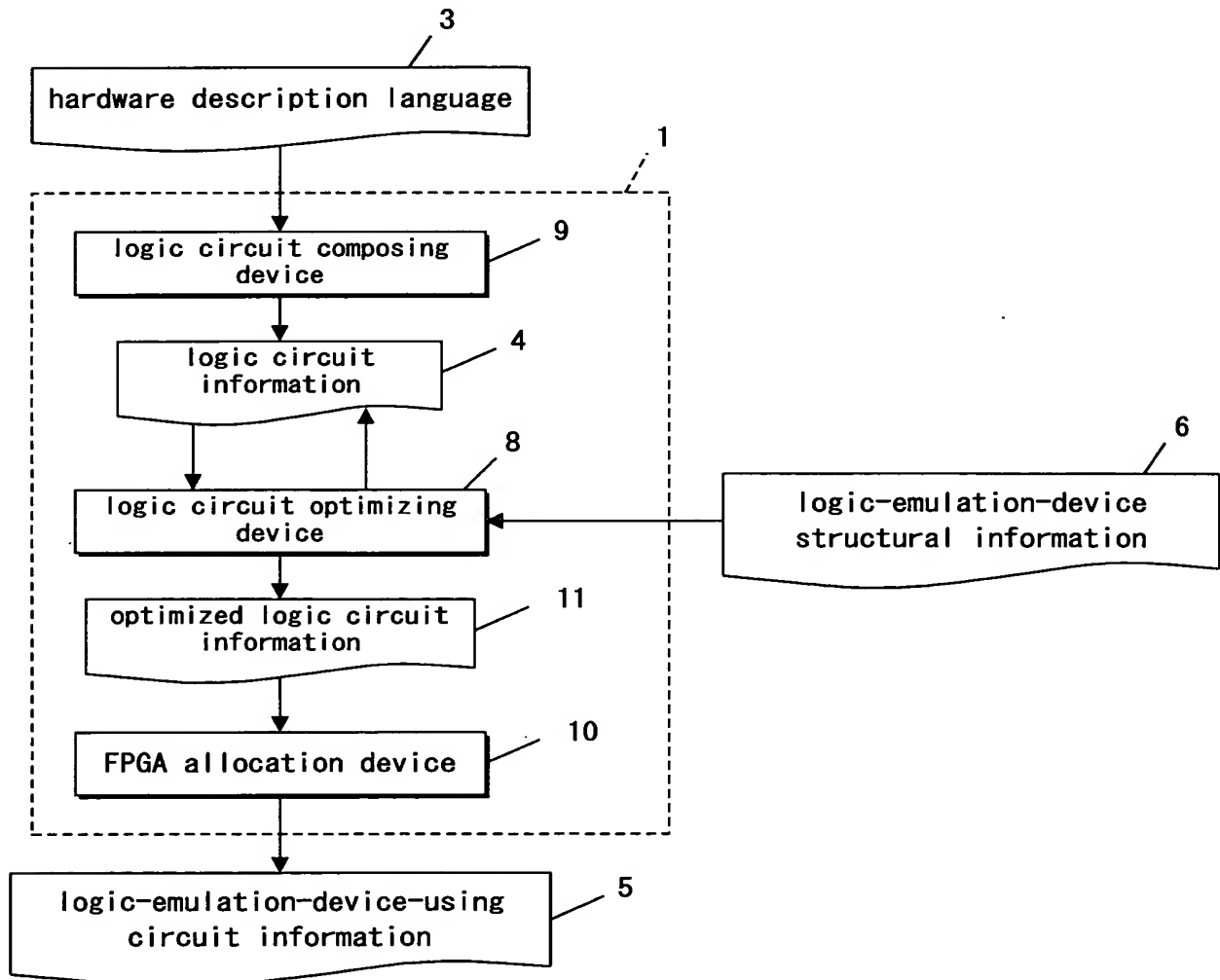
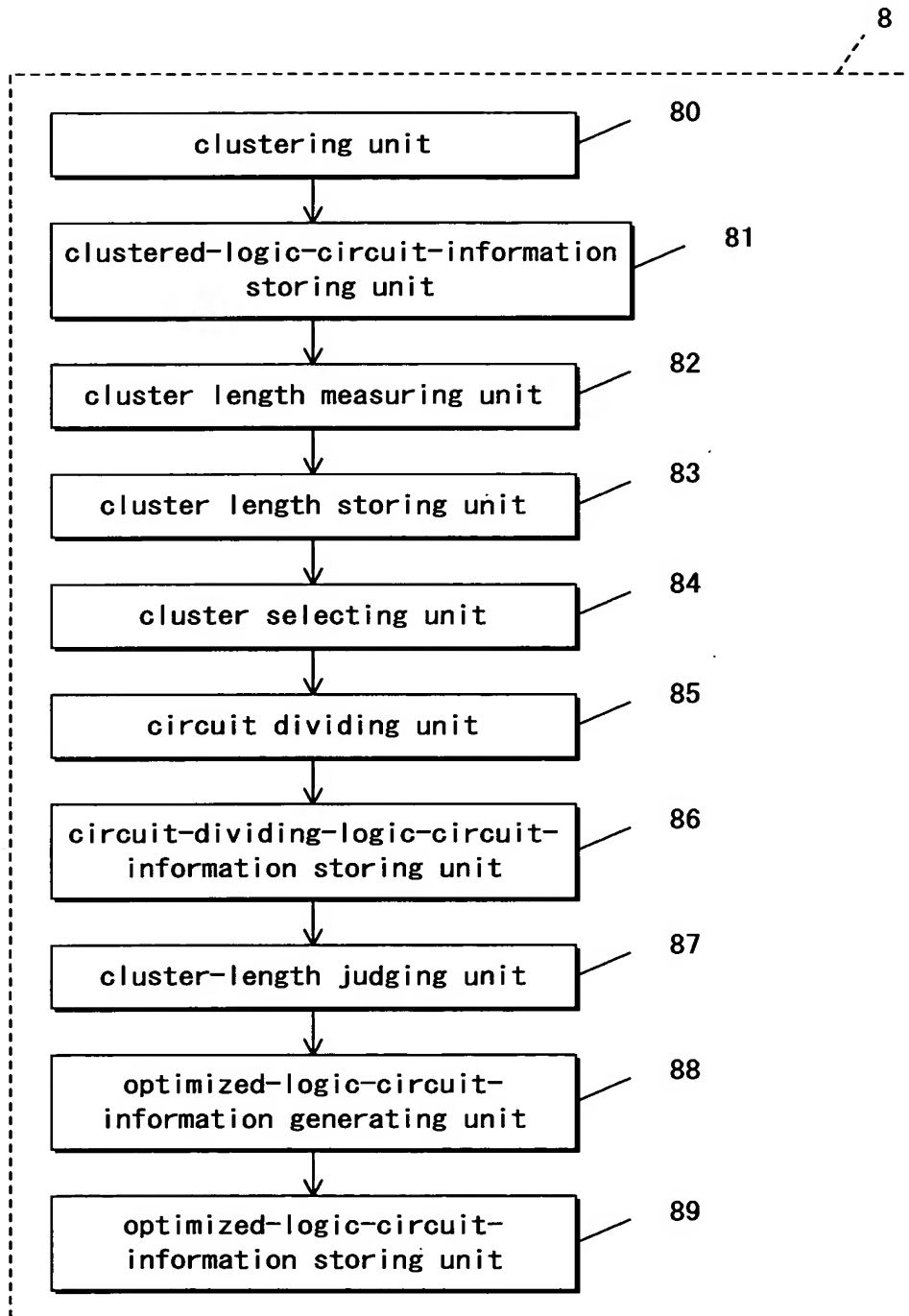


Fig. 3



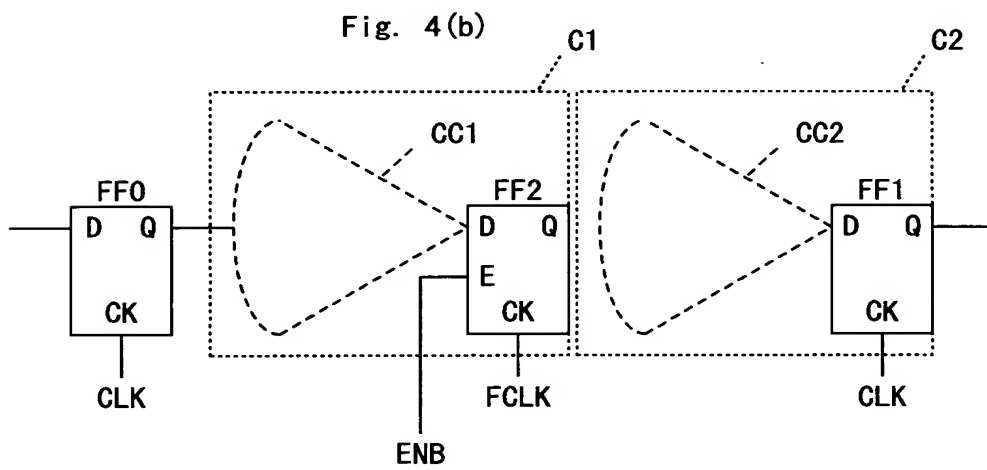
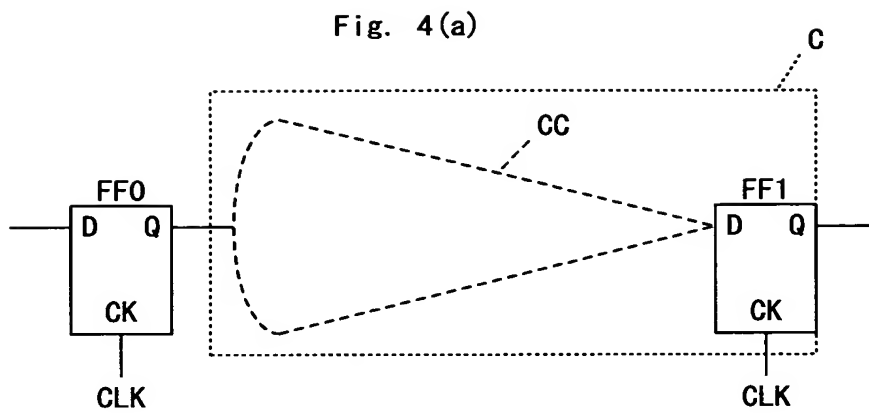


Fig. 5

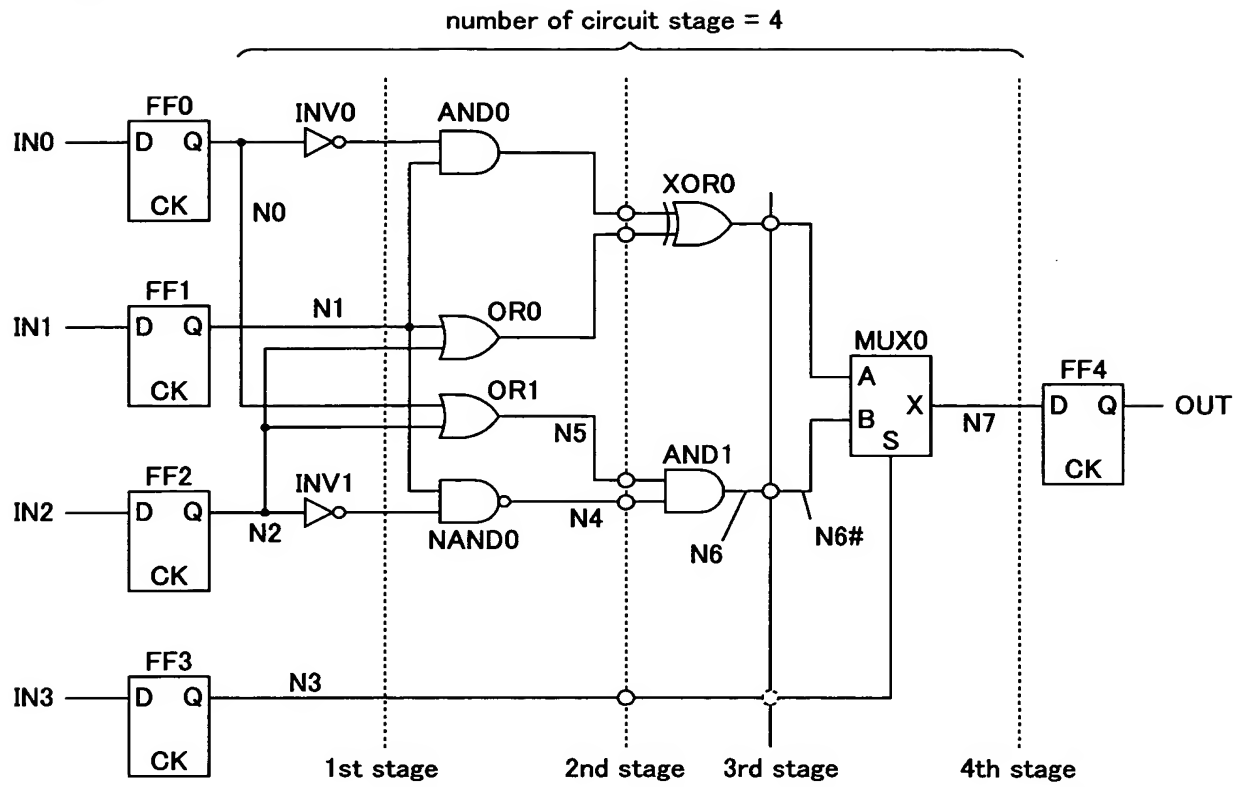


Fig. 6

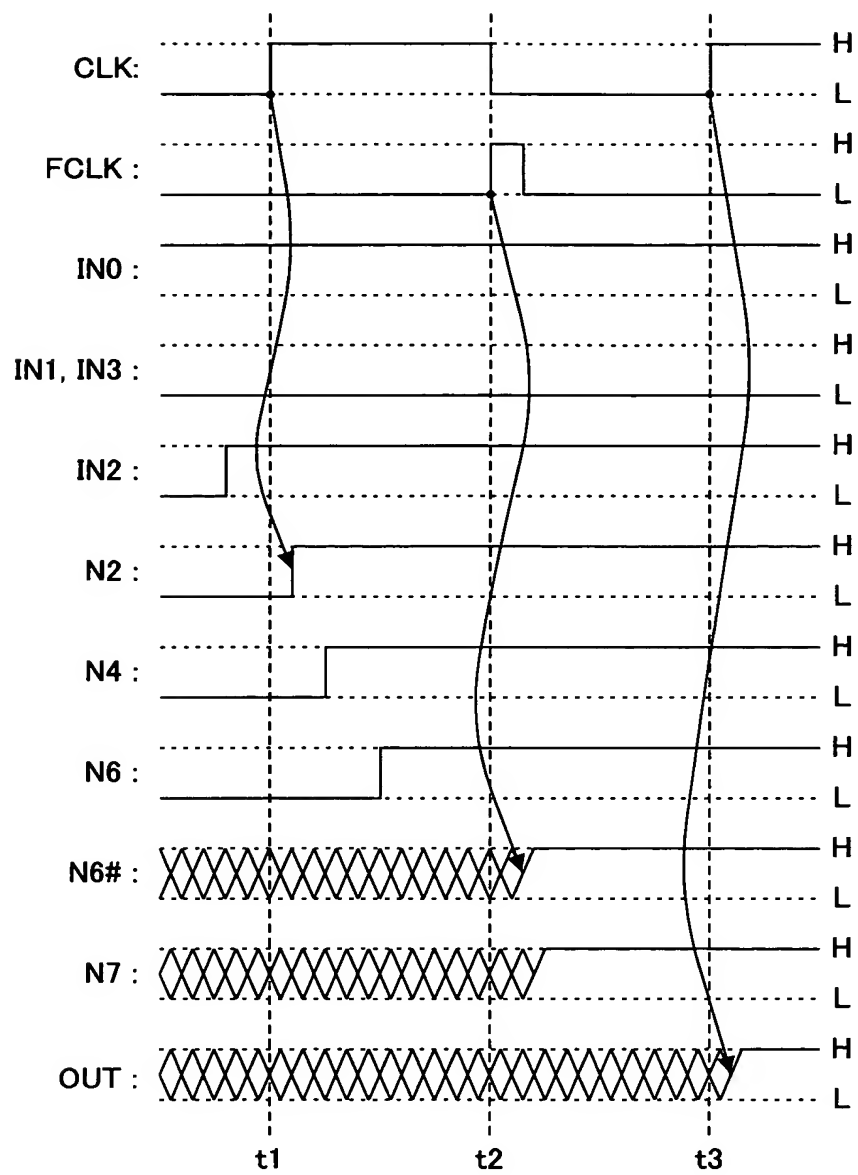


Fig. 7

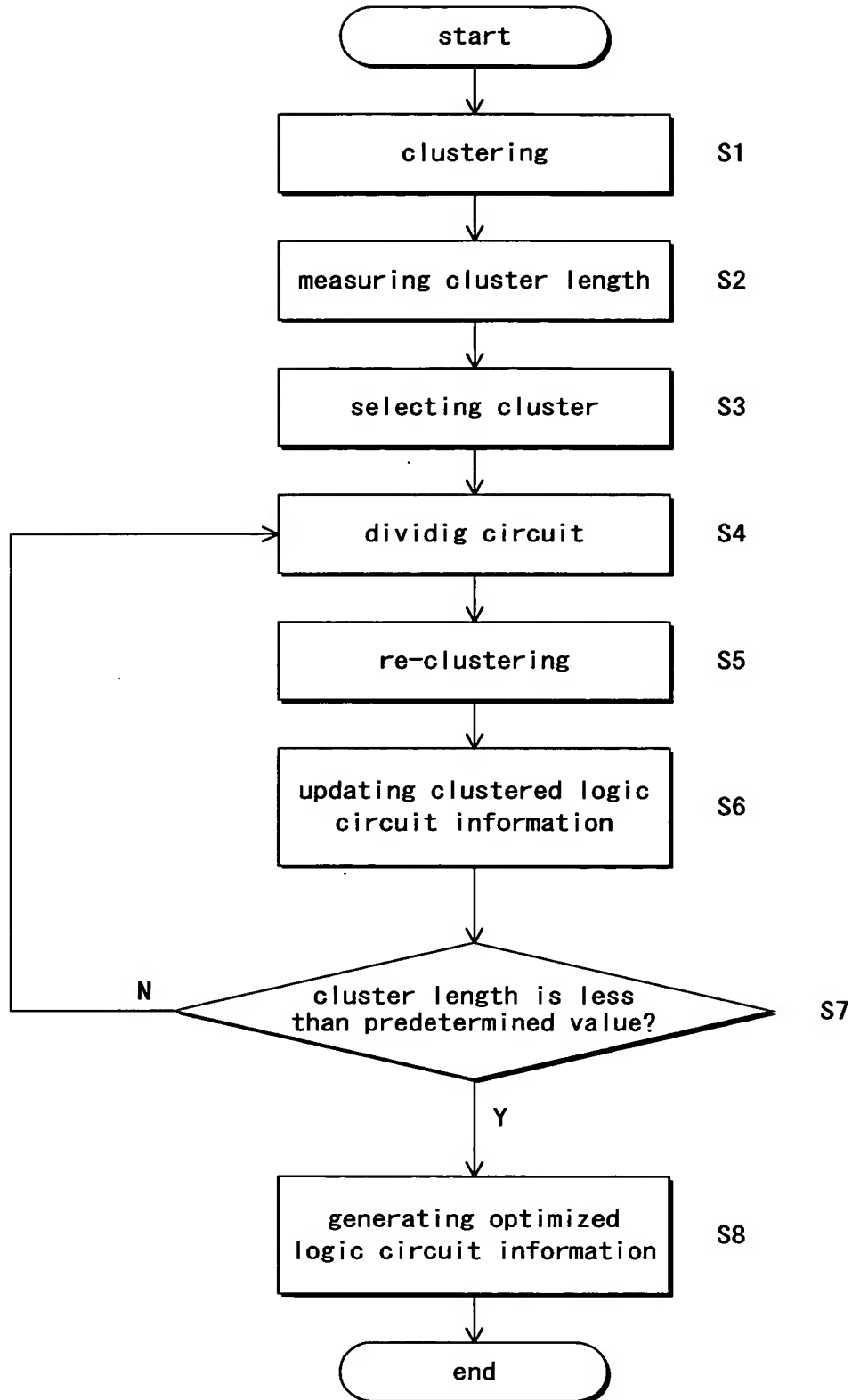


Fig. 8(a)

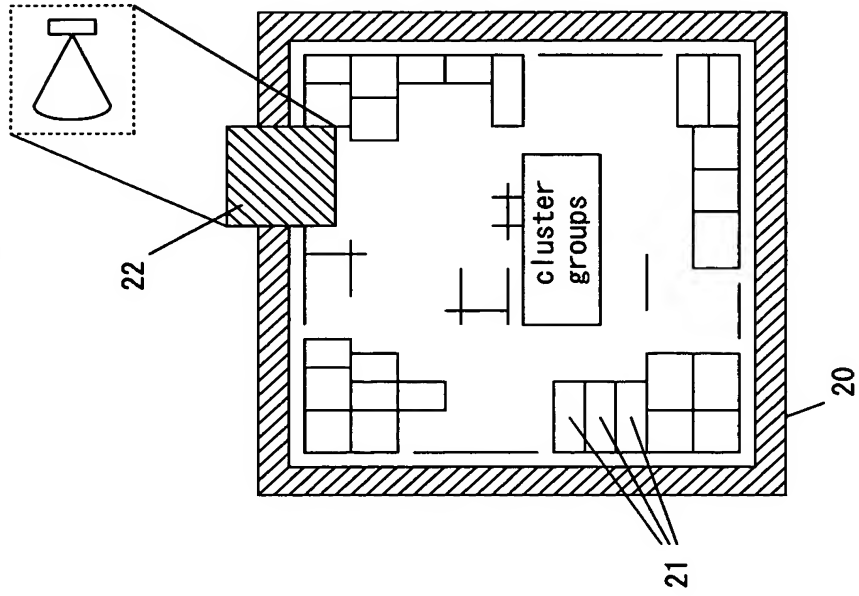


Fig. 8(b)

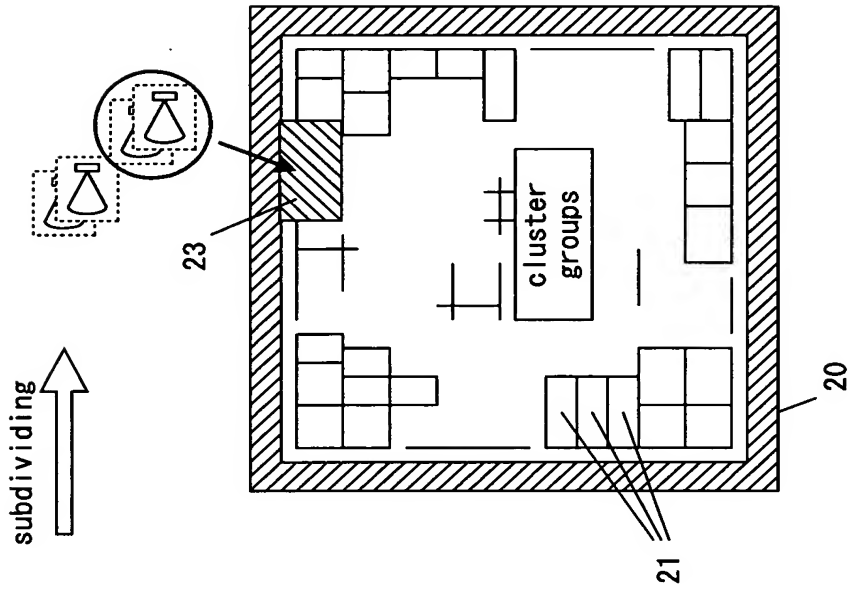


Fig. 9

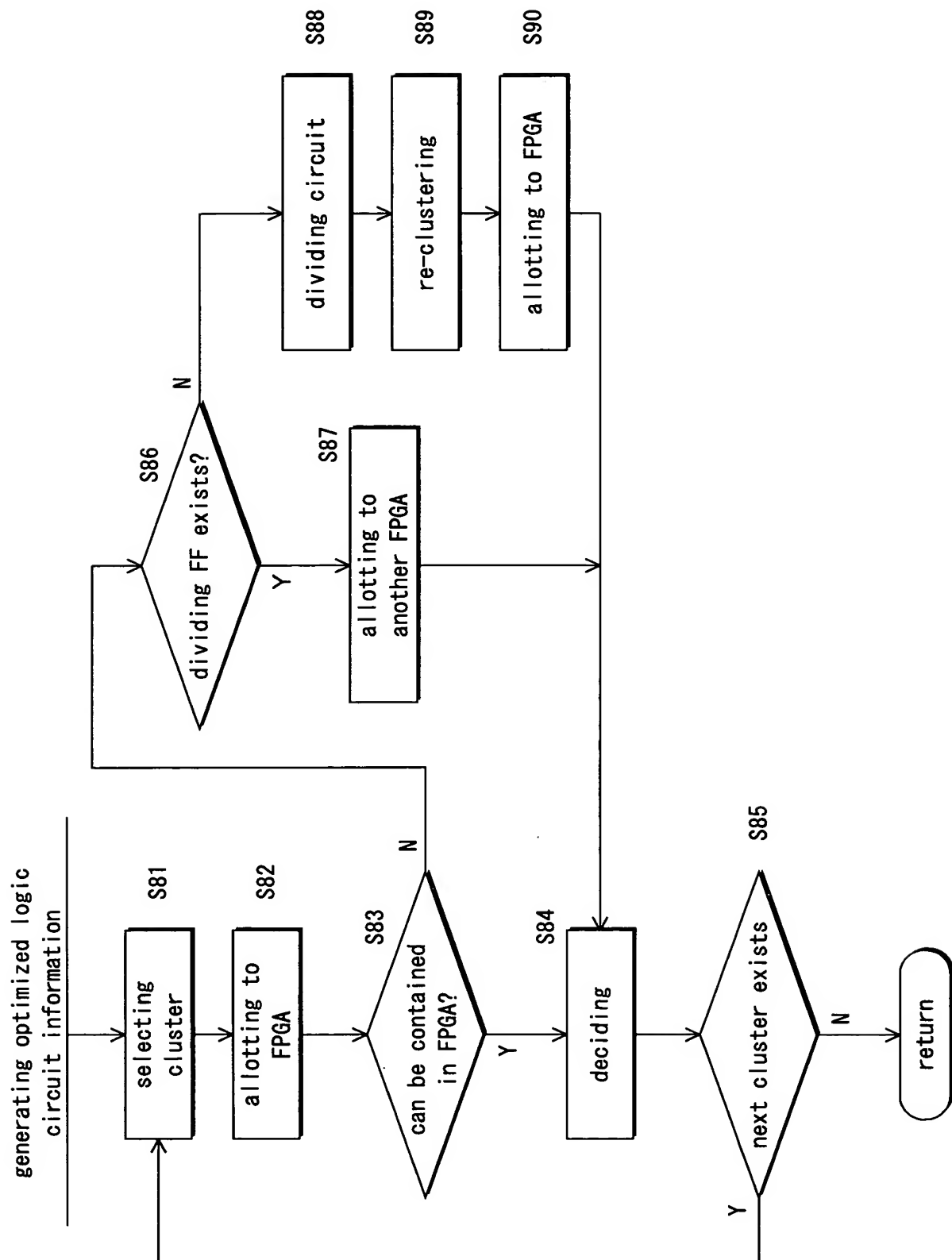


Fig. 10

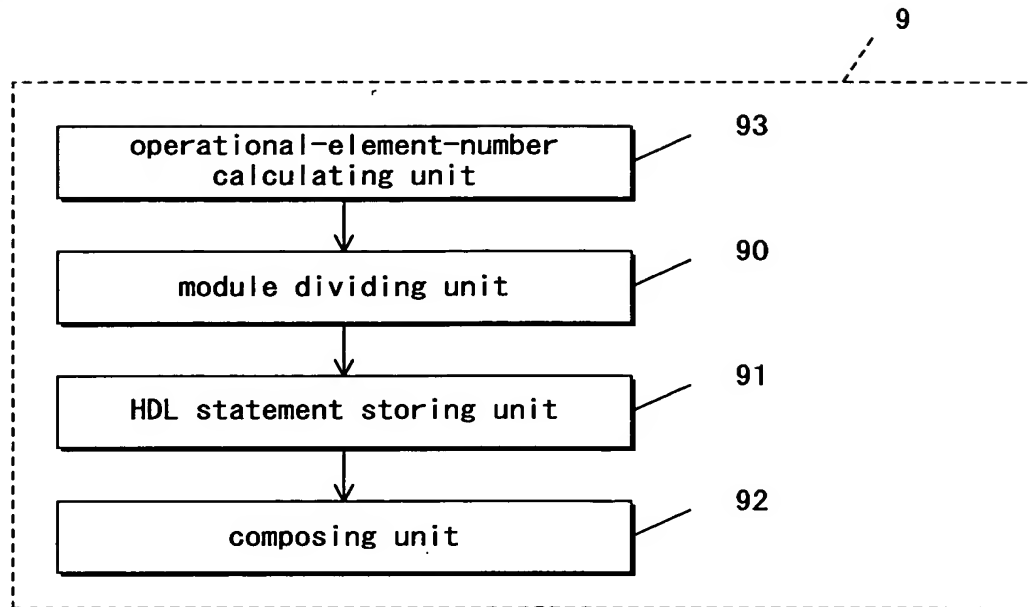


Fig. 11

```

module example_module(A,B,C,OUT)
input A,B,C;
output OUT;

```

```

    x=(A+B)*(A*B);

```

40

```

    case OUT(C)
        1'b0:OUT=x;
        1'b1:OUT≠ x;
    endcase

```

41

```

endmodule

```

Fig. 12

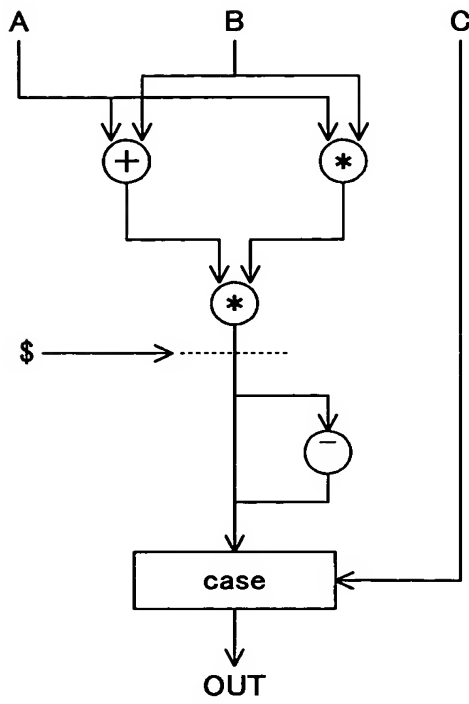


Fig. 13

```

module example_module(A,B,C,OUT)
input A,B,C;
output OUT;

```

```

    x=(A+B)*(A*B); 40
    always(negedge CLK) 42
    _x=x;
    case OUT(C) 41
    1'b0:OUT=_x;
    1'b1:OUT=~_x;
    endcase
endmodule

```

Fig. 14

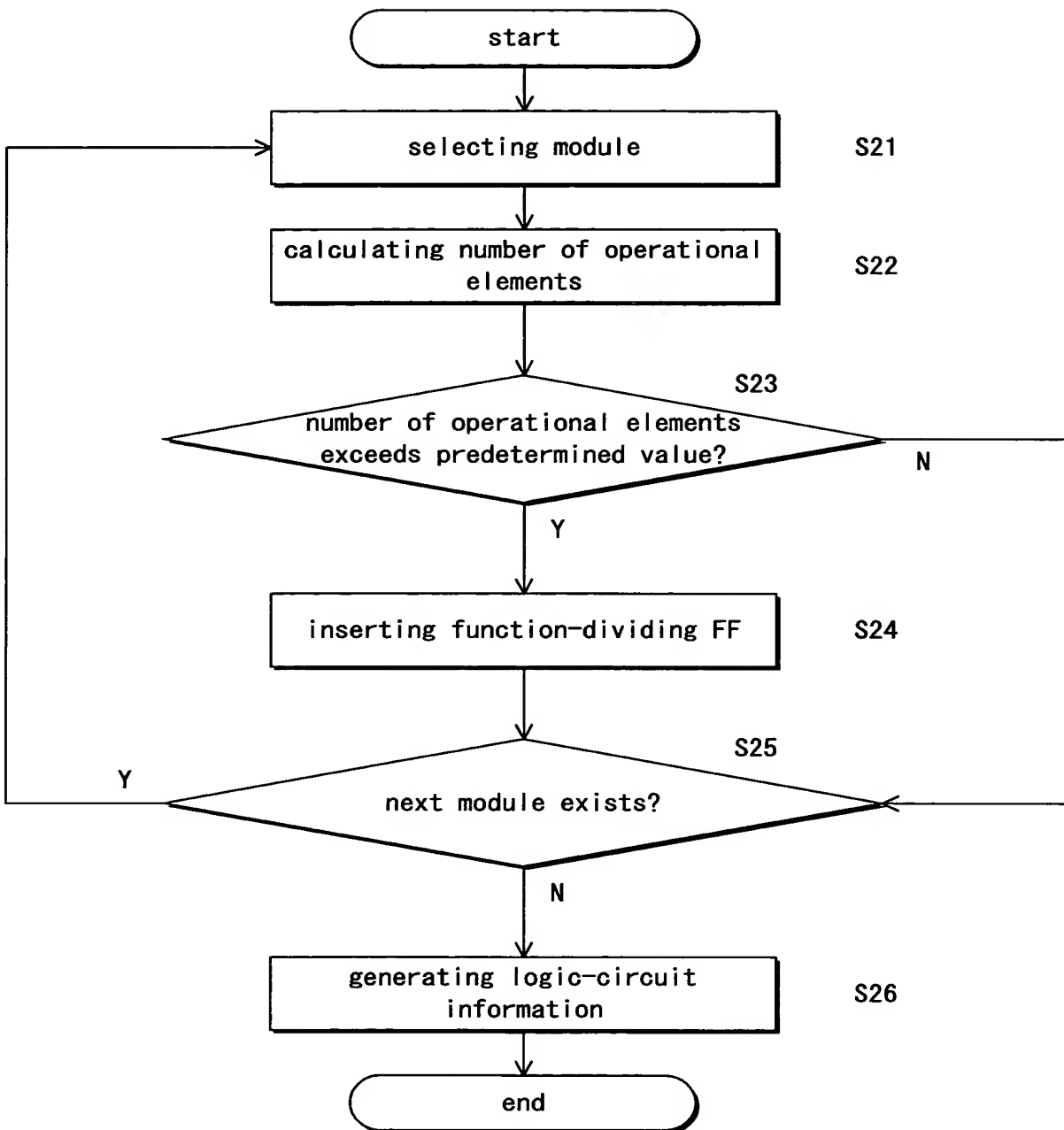


Fig. 15

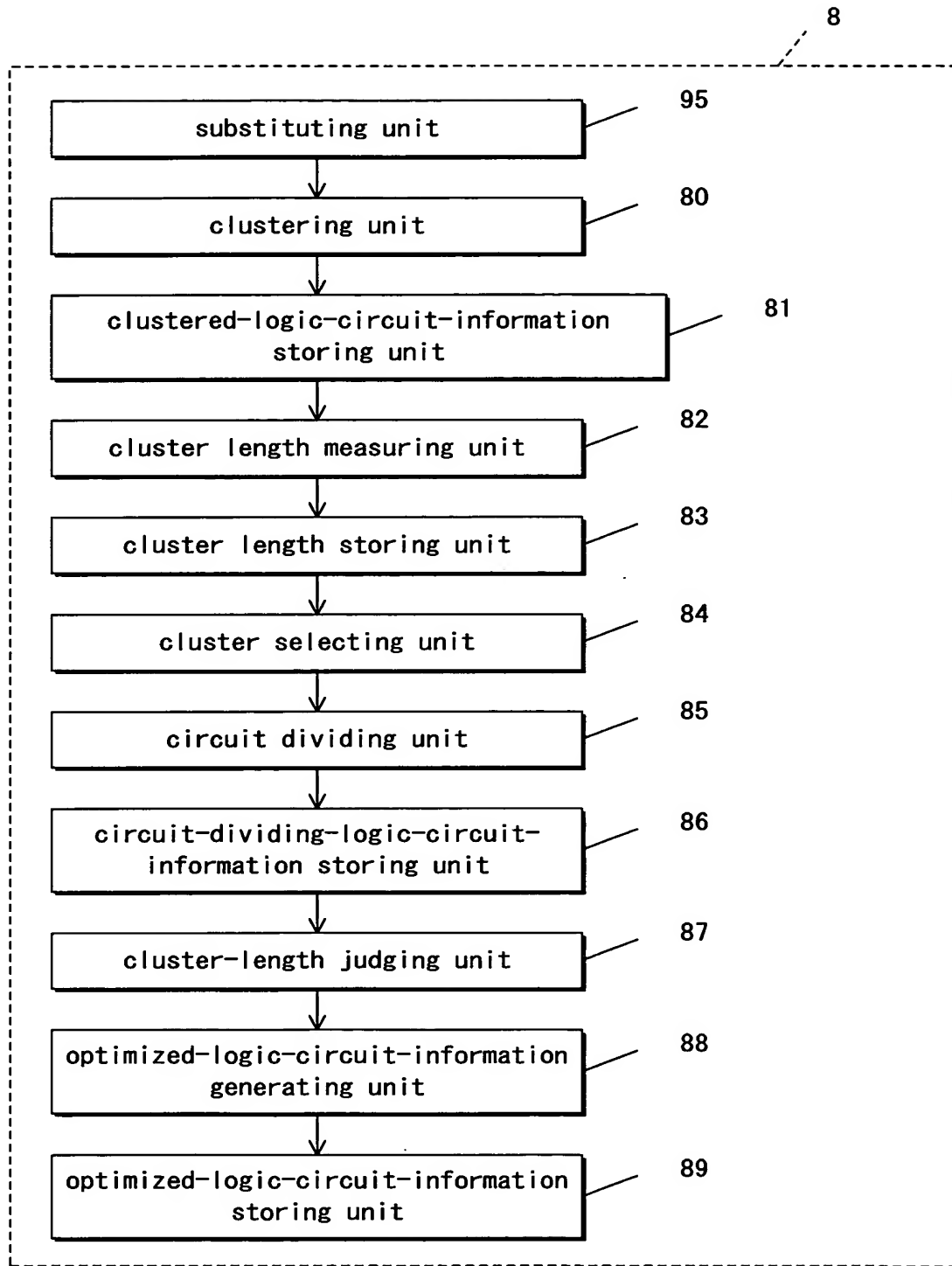


Fig. 16

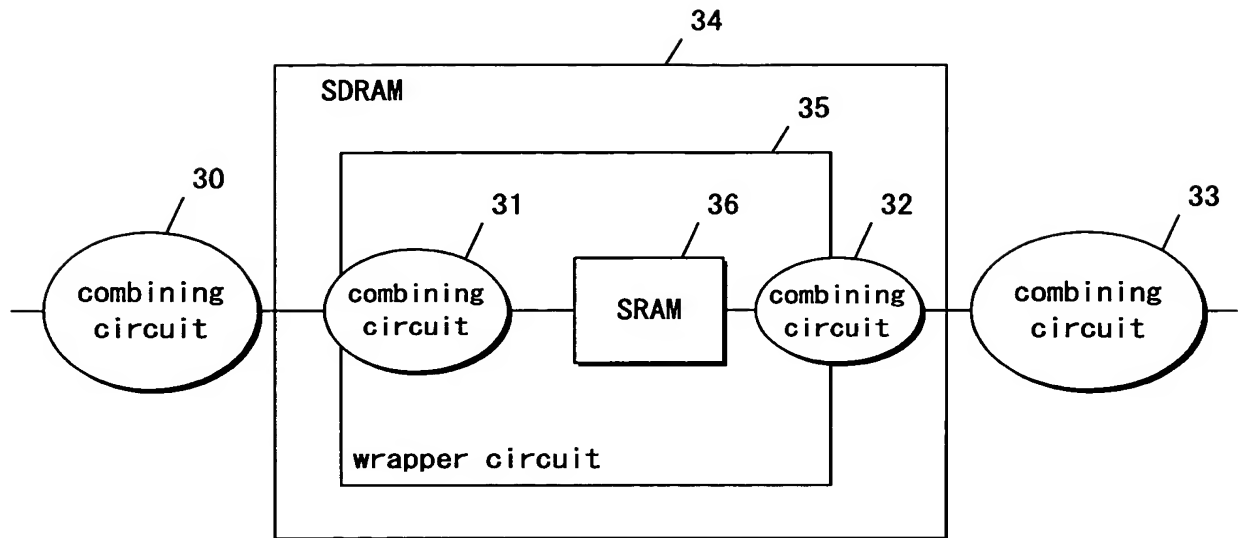


Fig. 17

kinds of memory	conversion value (number of circuit stages)
4Mbit SRAM	10
1Mbit SRAM	2

Fig. 18

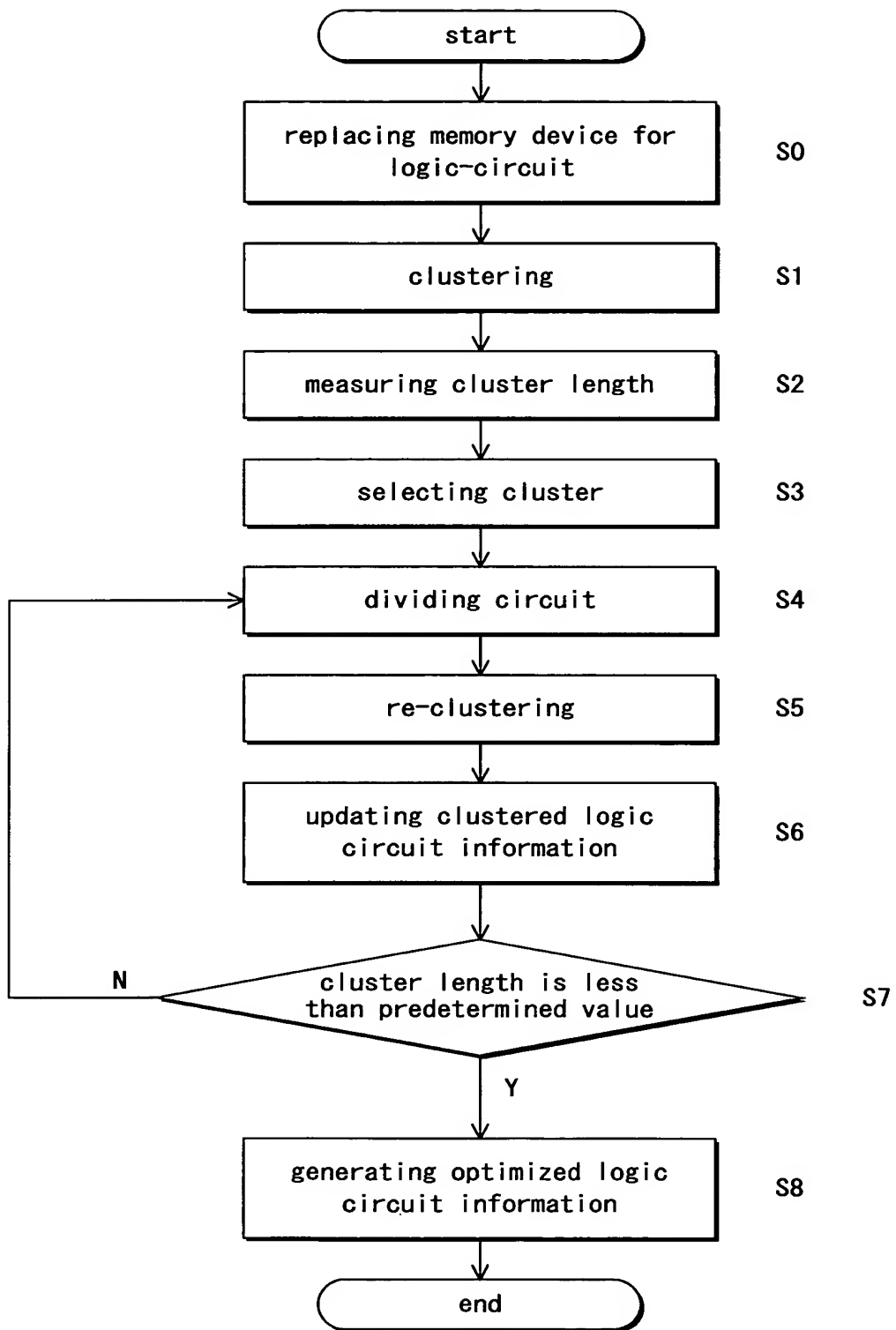


Fig. 19

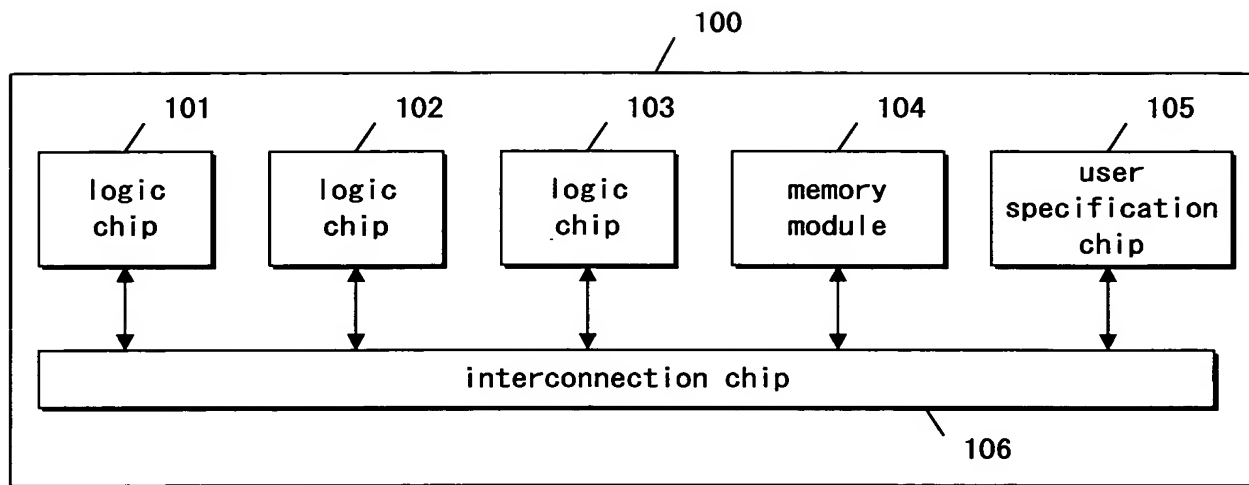


Fig. 20(a)

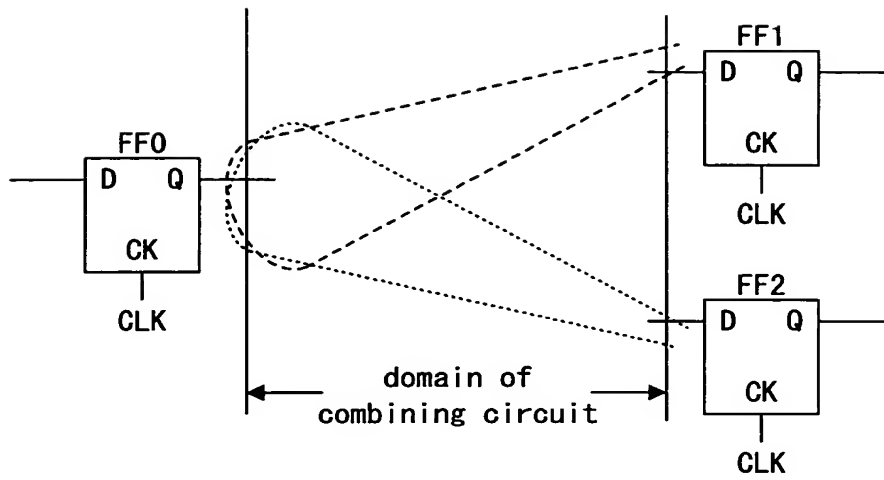


Fig. 20(b)

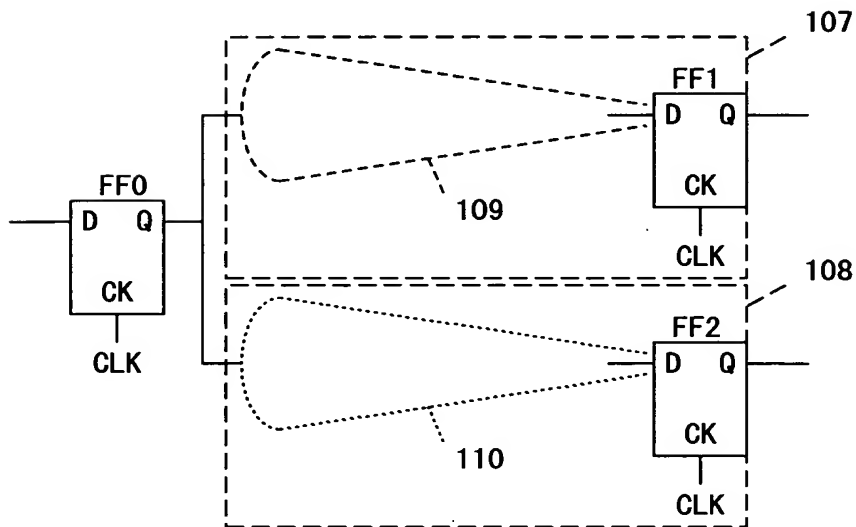


Fig. 21

